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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,306	04/01/2004	Katsuya Shinohara	56937-111	8591

7590 07/27/2006

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EXAMINER	
PATEL, SHAMBHAVI K	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,306	SHINOHARA, KATSUYA	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/01/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-8 are pending.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

2. The information disclosure statement filed 01 April 2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 6 and 7** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The meaning of claims 6 and 7 are unclear, and *the Examiner interprets claim 6 to be performing cycle-accurate simulation and claim 7 to be performing real-time simulation.*

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claim 1-8 are rejected** under 35 U.S.C. 102(b) as being clearly anticipated by **Ghosh et al. ('Methodology for Hardware/Software Co-Verification in C/C++)**, herein referred to as Ghosh.

Regarding claim 1:

Ghosh is directed to a simulator apparatus comprising:

a. a simulator model including a functional model for CPU constituting a system to be simulated **('Introduction' paragraph 7; section 3.1 'Bus Functional Model')**

b. a simulator model including a functional model for hardware to be connected to buses linked to the CPU **(section 2 'Design Flow' paragraph 2)**

c. plural types of interfaces included in the simulator models and enabling plural types of simulators for various uses to access to the functional models **(section 3.1.2 'Memory Mapped I/O' paragraphs 3-4)**

d. a simulator controlling device for selecting any of the plural types of the interfaces and accessing the respective functional models via the selected interfaces **(section 3.1.2 'Memory Mapped I/O' paragraphs 3-4)**

Regarding claim 2:

Ghosh is directed to a simulator apparatus as claimed in claim 1, wherein the interfaces for the respective functional models comprise an interface usable in a simulator for verifying software **('Introduction' paragraph 6; section 3.2 'Instruction Set Simulator')**.

Regarding claim 3:

Ghosh is directed to a simulator apparatus as claimed in claim 1, wherein the interfaces for the respective functional models comprise an interface usable in a simulator for verifying hardware **('Introduction' paragraph 6; section 3.2 'Instruction Set Simulator')**.

Regarding claim 4:

Ghosh is directed to a simulator apparatus as claimed in claim 1, wherein the interfaces for the respective functional models comprise an interface usable in a simulator for verifying a system **('Introduction' paragraph 6; section 3.2 'Instruction Set Simulator')**.

Regarding claim 5:

Ghosh is directed to a simulator apparatus as claimed in claim 1, wherein the interfaces for the respective functional models comprise an interface usable in debugging **(section 3.1.6 'Performance Estimation Functions' paragraph 2)**

Regarding claim 6:

Ghosh is directed to a simulator apparatus as claimed in claim 1, wherein an interface capable of simulating clock cycles of the system as precision at processing level is comprised **(section 3.1 'Bus Functional Model' paragraph 3)**.

Regarding claim 7:

Ghosh is directed to a simulator apparatus as claimed in claim 1, wherein an interface capable of simulating a simulation time for the system as precision at processing level is comprised **(section 3.1.5 'Timers and Serial Port'; section 4.1 'dw8051 bus functional model' paragraph 5)**.

Regarding claim 8:

Ghosh is directed to a simulator apparatus as claimed in claim 1, wherein the interfaces for the respective functional models comprise an interface for extension usable in performance analysis **(section 3.1.6 'Performance Estimation Functions' paragraph 2)**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKP

KAMINI SHAH
SUPERVISORY PATENT EXAMINER